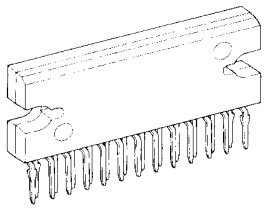
Preliminary TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6560HQ,TB6560FG

PWM Chopper-Type bipolar
Stepping Motor Driver IC

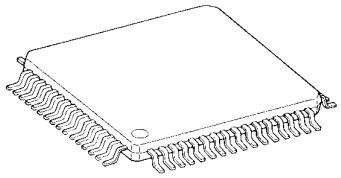
The TB6560HQ is a PWM chopper-type sinusoidal micro-step bipolar stepping motor driver IC.
It supports both 2-phase/1-2-phase/W1-2-phase/2W1-2-phase excitation mode and forward/reverse mode and is capable of low-vibration, high-performance drive of 2-phase bipolar type stepping motors using only a clock signal.

TB6560HQ



HZIP25-P-1.27

TB6560FG



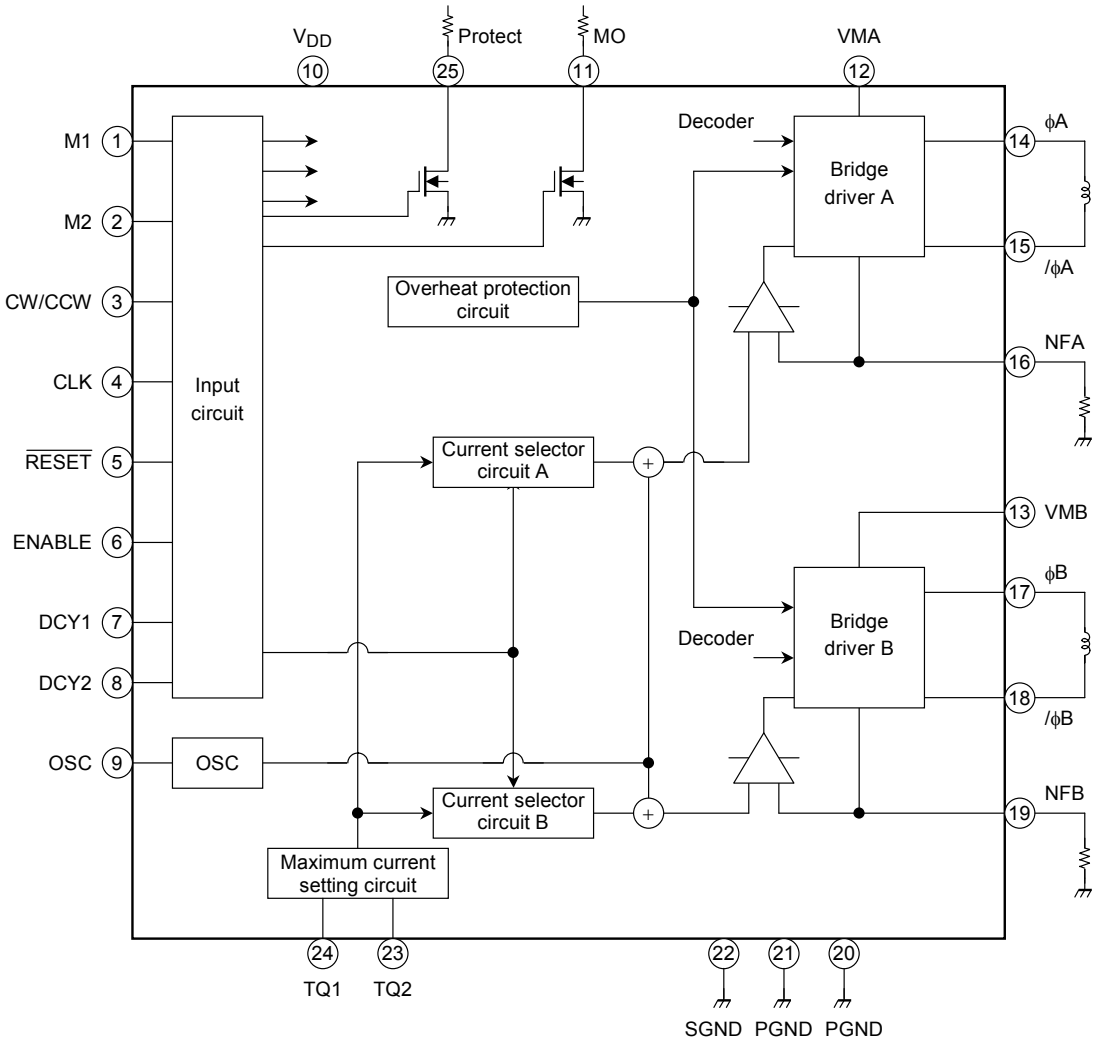
HQFP64-P-1010-0.50

Weight:
HZIP25-P-1.27: 9.86 g (typ.)
HQFP64-P-1010-0.50: 0.26 g (typ.)

Features

- Single-chip bipolar sinusoidal micro-step stepping motor driver
- Uses high withstand voltage BiCD process:
  Ron (upper + lower) = 0.75 Ω (typ.)
- Forward and reverse rotation control available
- Selectable phase drive (2, 1-2, W1-2, and 2W1-2)
- High output withstand voltage: V_{CEO} = 40 V
- High output current: I_{OUT} = HQ: 3.5 A (peak)
  FG: A (peak)
- Packages: HZIP25-P-1.27/HQFP64-P-1010-0.50
- Built-in input pull-down resistor: 200 kΩ (typ.)
- Output monitor pin equipped: MO current (I_{MO} (max) = 1 mA)
- Equipped with reset and enable pins
- Built-in overheat protection circuit

Block Diagram



Pin Functions (tentative pin numbering)

Pin No.		I/O	Symbol	Functional Description
HQ	FG			
1	10	Input	TQ2	Torque setting input (current setting) (built-in pull-down resistor)
2	9	Input	TQ1	Torque setting input (current setting) (built-in pull-down resistor)
3	12	Input	CLK	Step transition, clock input (built-in pull-down resistor)
4	16	Input	ENABLE	H: Enable; L: All output OFF (built-in pull-down resistor)
5	18	Input	$\overline{\text{RESET}}$	L: Reset (output is reset to its initial state) (built-in pull-down resistor)
6	19	—	SGND	Signal ground (control side)
7	20	—	OSC	Connects to and oscillates CR. Output chopping.
8	23	Input	V_{MB}	Motor side power pin (B phase side)
9	29	Output	$\overline{\text{OUT}}$_B	$\overline{\text{OUT}}$_B output
10	31	—	PGNDB	Power ground
11	34/35	—	N_{FB}	B channel output current detection pin (resistor connection). Short the two pins for FG.
12	39	Output	OUT_B	OUT_B output
13	42	Output	$\overline{\text{OUT}}$_A	$\overline{\text{OUT}}$_A output
14	45/46	—	N_{FA}	A channel output current detection pin (resistor connection). Short the two pins for FG.
15	48	—	PGNDA	Power ground
16	52	Output	OUT_A	OUT_A output
17	58	Input	V_{MA}	Motor side power pin (A phase side)
18	61	Output	M_O	Initial state detection output. ON when in initial state (open drain).
19	62	Output	Protect	When TSD, ON (open drain). Normal Z.
20	63	Input	V_{DD}	Control side power pin.
21	64	Input	CW/CCW	Forward/Reverse toggle pin. L: Forward; H: Reverse (built-in pull-down resistor)
22	1	Input	M2	Excitation mode setting input (built-in pull-down resistor)
23	2	Input	M1	Excitation mode setting input (built-in pull-down resistor)
24	3	Input	DCY2	Current Decay mode setting input (built-in pull-down resistor)
25	4	Input	DCY1	Current Decay mode setting input (built-in pull-down resistor)

HQ: No NC

FG: Other than the above pins, all are NC

Pull-down resistor 200 k Ω (typ.): [all control input pins]

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Power supply voltage		V_{DD}	6	V
		$V_{MA/B}$	40	V
Output current	Peak	$I_{O\ (PEAK)}$	3.5	A/phase
MO drain current		$I_{(MO)}$	1	mA
Input voltage		V_{IN}	5.5	V
Power dissipation		P_D	5 (Note 1)	W
			43 (Note 2)	
Operating temperature		T_{opr}	−30~85	°C
Storage temperature		T_{stg}	−55~150	°C

Note 1: No heat sink.

Note 2: Tc = 85°C

Recommended Operating Conditions (Ta = –20 to 85°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	$V_{MA/B}$	$V_{MA/B} \geqq V_{DD}$	4.5	—	26.4	V
Output current	I_{OUT}	—	—	—	3	A
Input voltage	V_{IN}	—	0	—	5.5	V
Clock frequency	f_{CLK}	—	—	—	15	kHz
OSC frequency	f_{OSC}	—	—	—	(600)	kHz

Electrical Characteristics (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Design Confirmation Conditions (Ta = –30 to 85°C, V_{DD} = 4.5 to 5.5 V, V_M = 4.5 to 26.4 V)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	High	$V_{IN\ (H)}$	1	M1, M2, CW/CCW, CLK, $\overline{RESET}$, ENABLE, DECAY, TQ1, TQ2, ISD	2.0	—	V_{DD}	V
	Low	$V_{IN\ (L)}$			–0.3	—	0.8	
Input hysteresis voltage		V_H			—	600	—	mV
Input current		$I_{IN\ (H)}$	1	M1, M2, CW/CCW, CLK, $\overline{RESET}$, ENABLE, DECAY, TQ1, TQ2, ISD V_{IN} = 5.0 V Built-in pull-down resistor	15	25	35	μA
		$I_{IN\ (L)}$		V_{IN} = 0 V	—	—	1	μA
Consumption current V_{DD} pin		I_{DD1}	1	Output open, $\overline{RESET}$: H, ENABLE: H (2, 1-2 phase excitation)	—	5	10	mA
		I_{DD2}		Output open, $\overline{RESET}$: H, ENABLE: H (W1−2, 2W1-2 phase excitation)	—	5	10	
		I_{DD3}		$\overline{RESET}$: L, ENABLE: L	—	4	5	
		I_{DD4}		$\overline{RESET}$: H, ENABLE: L	—	4	5	
Output channel margin of error		ΔV_O	—	B/A, C_{OSC} = 0.0033 μF	–5	—	5	%
V_{NF} level Level differential		V_{NFHH}	—	TQ1 = H, TQ2 = H	10	20	30	%
		V_{NFHL}		TQ1 = L, TQ2 = H	47	50	53	
		V_{NFLH}		TQ1 = H, TQ2 = L	72	75	78	
		V_{NFLL}		TQ1 = L, TQ2 = L			100	
Minimum clock pulse width		$t_{W\ (CLK)}$	—	—	—	100	—	ns
MO output residual voltage		V_{OL} MO	—	I_{OL} = 1 mA	—	—	0.5	V
TSD		TSD	—	(Design target value)	150	170	190	°C
TSD hysteresis		TSDhys	—	(Design target value)	—	20	—	°C
Oscillating frequency		f_{OSC}		C = 330 pF	91	130	169	kHz
MO drain current		$I_{(MO)}$					1	mA

Electrical Characteristics (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V)

Design Confirmation Conditions (Ta = –30 to 85°C, V_{DD} = 4.5 to 5.5 V, V_M = 4.5 to 26.4 V)

Output Block

Characteristic				Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output transistor ON resistor			Upper side	Ron_{U1}	4	Forward direction I_{OUT} = 1.5 A		—	0.35	0.45	Ω
			Lower side	Ron_{L1}				—	0.4	0.55	
			Upper side	Ron_{U2}		Reverse direction I_{OUT} = 1.5 A		—	0.35	0.45	
			Lower side	Ron_{L2}				—	0.4	0.55	
Output dark current (A + B Channels)				I_{M1}	2	$\overline{ENABLE}$: "L" level, output open $\overline{RESET}$: "L" level		—	—	50	μA
				I_{M2}		$\overline{ENABLE}$: "H" level, output open $\overline{RESET}$: "H" level		—	8	10	mA
A-B chopping current (Note)	2W1-2-phase excitation	W1-2-phase excitation	1-2-phase excitation	Vector	—	θ = 0	TQ1 = L, TQ2 = L	—	100	—	%
	2W1-2-phase excitation	—	—			θ = 1/8		93	98	100	
	2W1-2-phase excitation	W1-2-phase excitation	—			θ = 2/8		87	92	97	
	2W1-2-phase excitation	—	—			θ = 3/8		78	83	88	
	2W1-2-phase excitation	W1-2-phase excitation	1-2-phase excitation			θ = 4/8		66	71	76	
	2W1-2-phase excitation	—	—			θ = 5/8		51	56	61	
	2W1-2-phase excitation	W1-2-phase excitation	—			θ = 6/8		33	38	43	
	2W1-2-phase excitation	—	—			θ = 7/8		15	20	25	
	2-phase excitation					—		—	100	—	

Note: Maximum current (θ = 0): 100%

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Reference voltage		ΔV_{NF}	—	TQ1, 2 = L (100%) OSC = 100 kHz	—	(500)	—	mV
Output transistor switching characteristics		t_r	7	R_L = 2 Ω, V_{NF} = 0 V, C_L = 15 pF	—	0.1	—	μs
		t_f			—	0.1	—	
Delay time		t_{pLH}		CLK to output	—	1	—	
		t_{pHL}			—	2	—	
		t_{pLH}		CK to output	—	0.5	—	
		t_{pHL}			—	1	—	
		t_{pLH}		$\overline{\text{RESET}}$ to output	—	2.0	—	
		t_{pHL}			—	2.5	—	
		t_{pLH}		ENABLE to output	—	5.0	—	
		t_{pHL}			—	6.0	—	
Output leakage current	Upper side	I_{LH}	6	V_M = 40 V	—	—	10	μA
	Lower side	I_{LL}			—	—	10	

Description of Functions

1. Excitation Settings

You can use the M1 and M2 pin settings to configure four different excitation settings. (The default is 2-phase excitation using the internal pull-down.)

Input		Mode (Excitation)
M2	M1	
L	L	2-phase
L	H	1-2-phase
H	L	W1-2-phase
H	H	2W1-2-phase

2. Function

You can change the output to OFF and Initial mode by using the ENABLE and $\overline{\text{RESET}}$ pins respectively.
In Initial mode, the CLK and CW/CCW settings don't matter.

Input				Output Mode
CLK	CW/CCW	$\overline{\text{RESET}}$	ENABLE	
↓	L	H	H	CW
↓	H	H	H	CCW
X	X	L	H	Initial mode
X	X	X	L	Z

X: Don't care

3. Initial Mode

When $\overline{\text{RESET}}$ is used, the phase currents are as follows. In this instance, the MO pin is L (connected to open drain).

Excitation Mode	A Phase Current	B Phase Current
2-phase	100%	−100%
1-2-phase	100%	0%
W1-2-phase	100%	0%
2W1-2-phase	100%	0%

4. Current Decay Settings

Output is generated by four PWM blasts; 25% decay is created by inducing decay during the last blast in Fast mode; 50% decay is created by inducing decay during the last two blasts in Fast mode; and 100% decay is created by inducing all four blasts in Fast mode.

If there is no input with the pull-down resistor connection then the setting is Normal.

Dcy2	Dcy1	Current Decay Setting
L	L	Normal 0%
L	H	25% Decay 25%
H	L	50% Decay 50%
H	H	100% Decay 100%

5. Torque Settings (Current Value)

The current ratio used in actual operations is determined in regard to the current setting due to resistance. Configure this for extremely low torque scenarios such as when Weak Excitation mode is stopped.

If there is no input with the pull-down resistor connection then the setting is 100% torque.

TQ2	TQ1	Current Ratio
L	L	100%
L	H	75%
H	L	50%
H	H	20% (weak excitation)

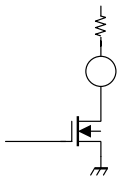
6. Protect and MO (Output Pins)

You can configure settings from the receiving side by using an open drain connection for the output pins and making the pull-up voltage variable.

When a given pin is in its designated state it will go ON and output at Low level.

Pin State	Protect	MO
Low	Overheat protection operation	Initial state
Z	Normal operation	Other than initial state

Open-drain connection



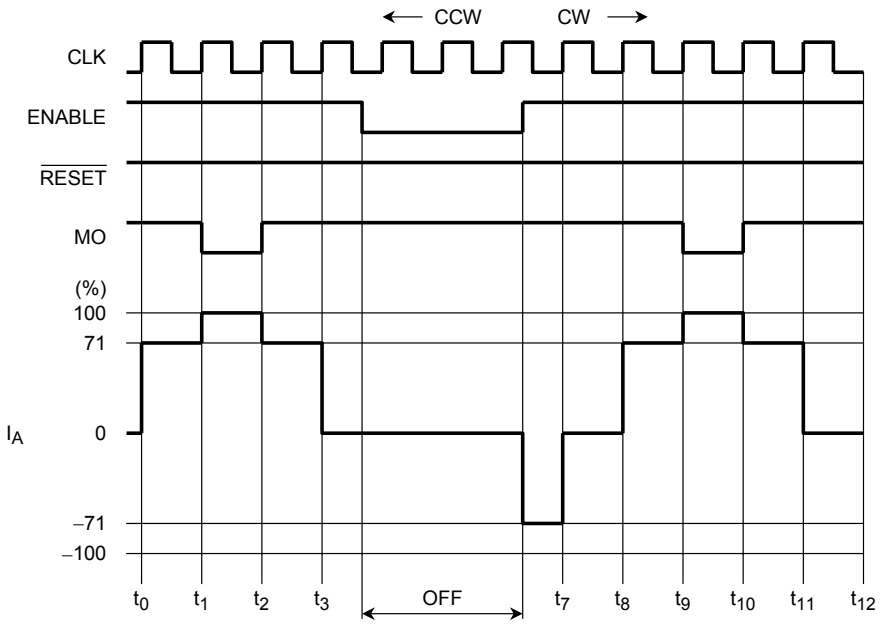
7. OSC

Output chopping waves are generated by connecting the condenser and having the CR oscillate. The values are as shown below (roughly: ± 30% margin of error).

Condenser	Oscillating Frequency
1000 pF	44 kHz
330 pF	130 kHz
100 pF	400 kHz

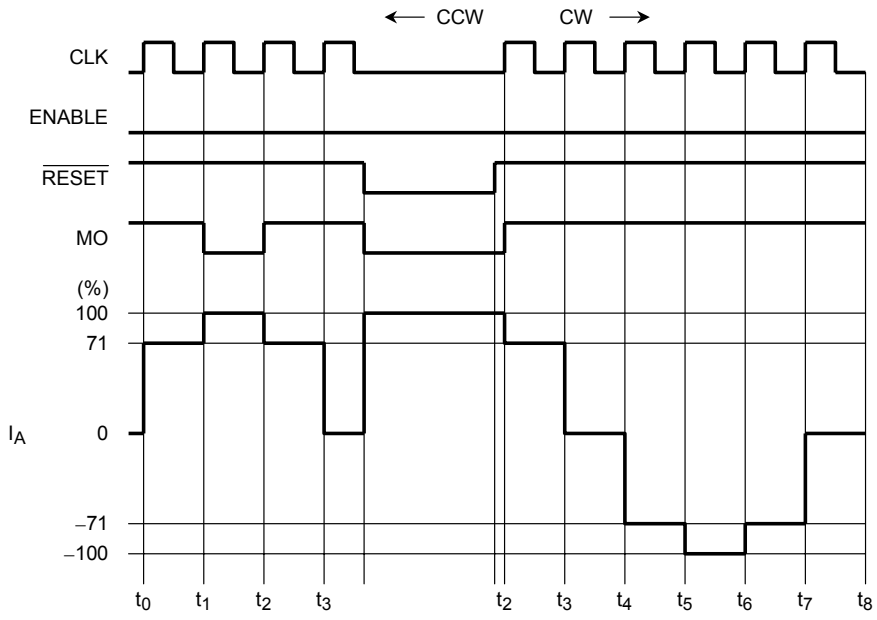
Relationship between Enable, $\overline{\text{RESET}}$ and Output (OUT and MO)

Ex-1: ENABLE 1-2-Phase Excitation (M1: H, M2: L)



The ENABLE signal at Low level disables only the output signals. Internal logic functions proceed in accordance with input clock signals and without regard to the ENABLE signal. Therefore output current is initiated by the timing of the internal logic circuit after release of disable mode.

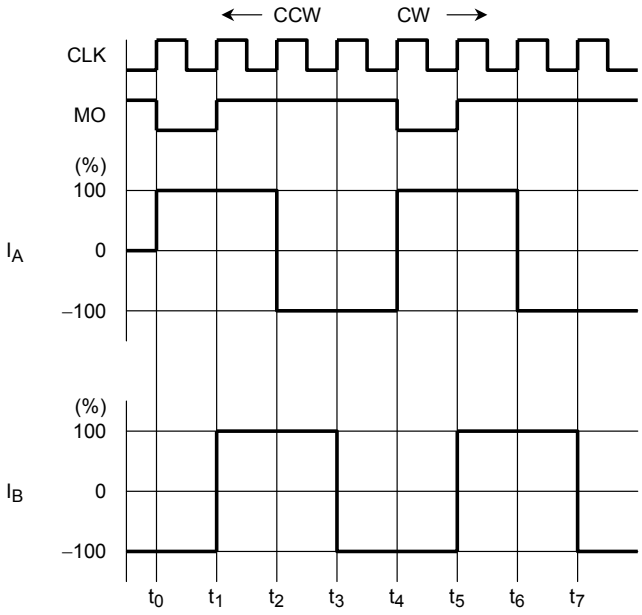
Ex-2: $\overline{\text{RESET}}$ 1-2-Phase Excitation (M1: H, M2: L)



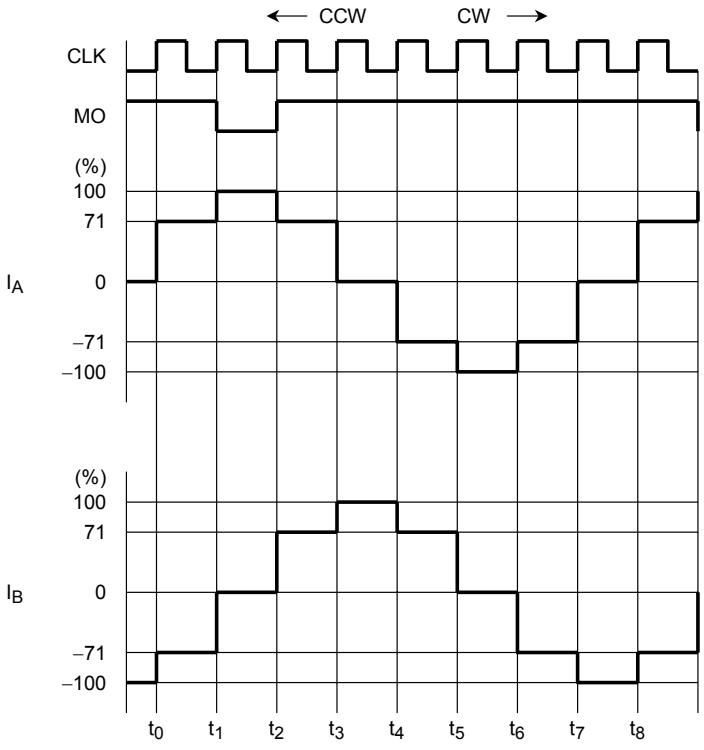
When the $\overline{\text{RESET}}$ signal goes Low level, output goes Initial state and the MO output goes Low level (Initial state: A Channel output current is 100%).

Once the $\overline{\text{RESET}}$ signal returns to High level, output continues from the next state after Initial from the next raise in the Clock signal.

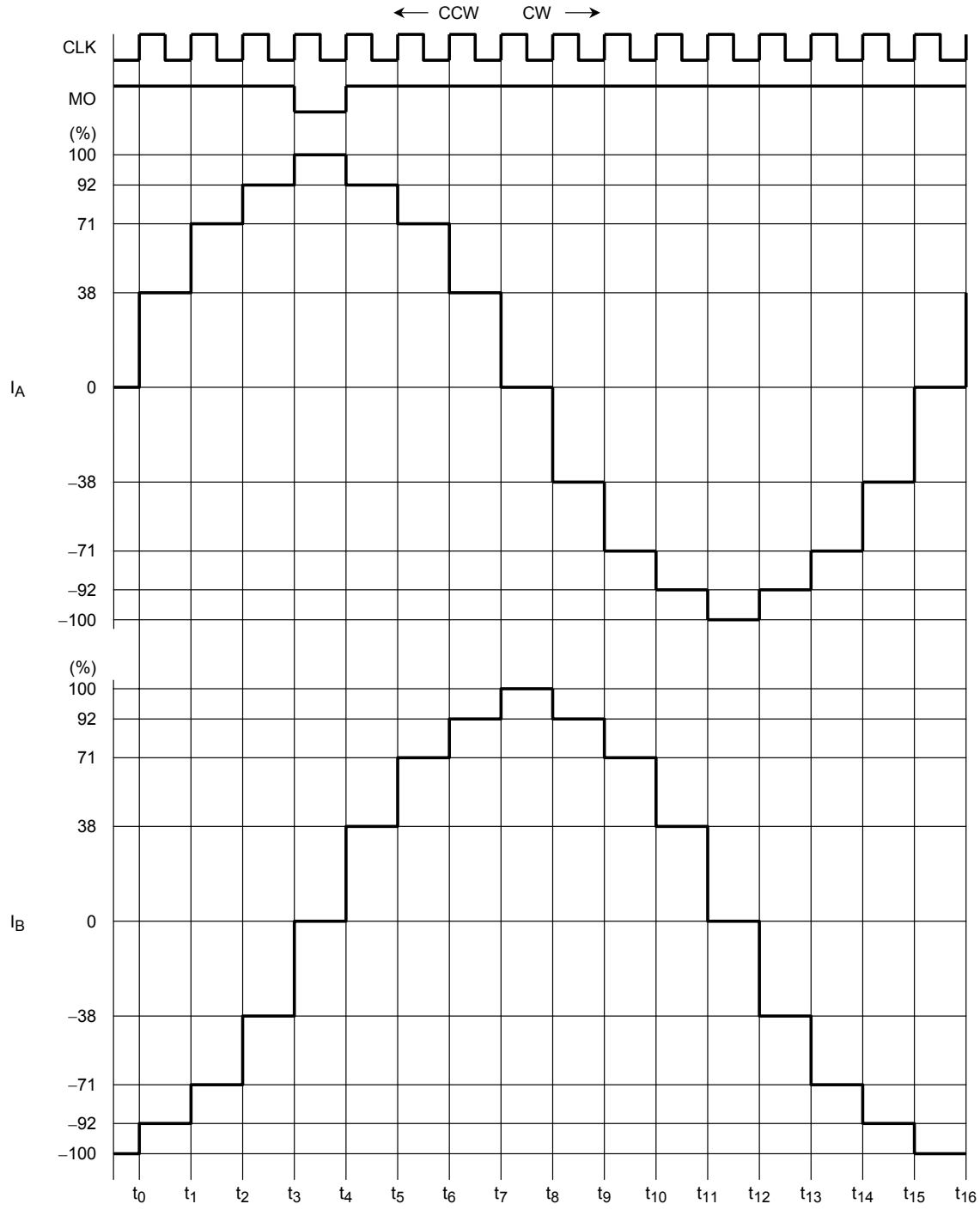
2-Phase Excitation (M1: L, M2: L, CW Mode)



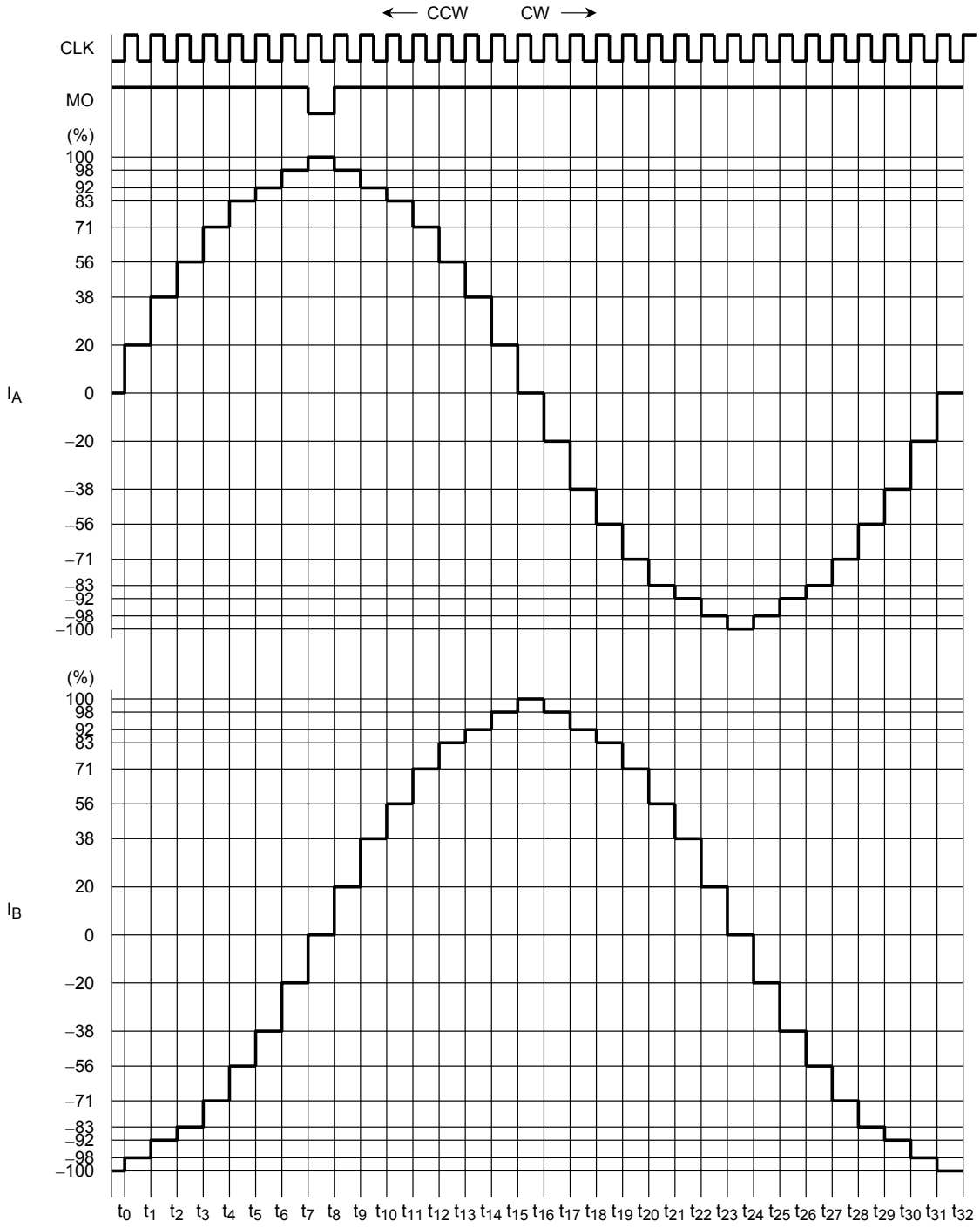
1-2-Phase Excitation (M1: H, M2: L, CW Mode)



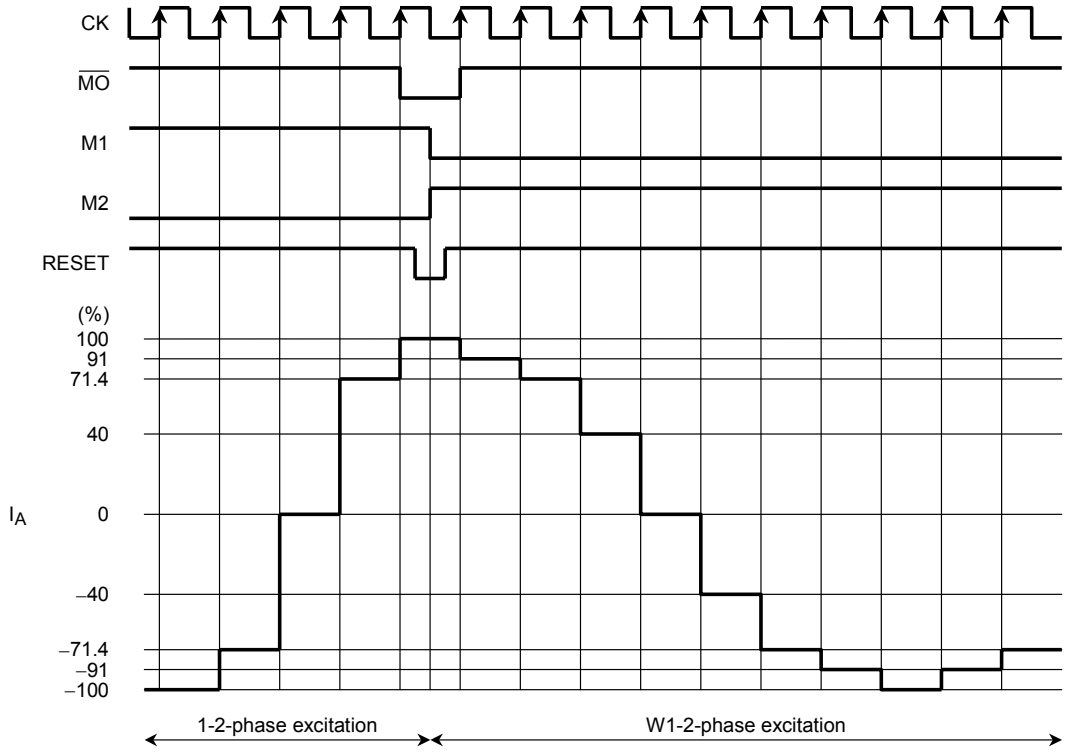
W1-2-Phase Excitation (M1: L, M2: H, CW Mode)



2W1-2-Phase Excitation (M1: H, M2: H, CW Mode)



<Input Signal Example>

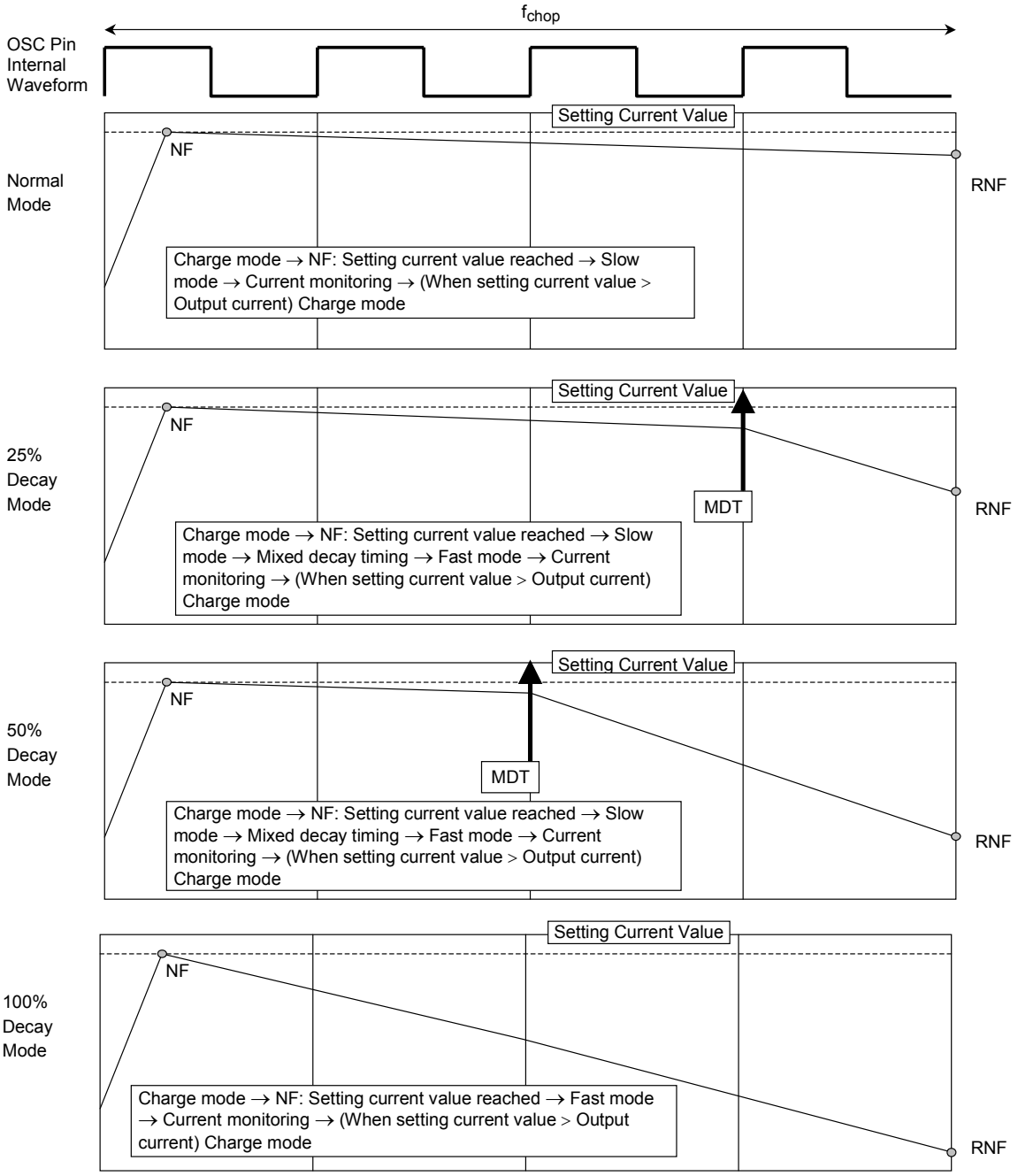


1. Current Waveform and Settings of Mixed Decay Mode

You can configure the points of the current's shaped width (current's pulsating flow) using 1bit input in Decay mode for constant-current control.

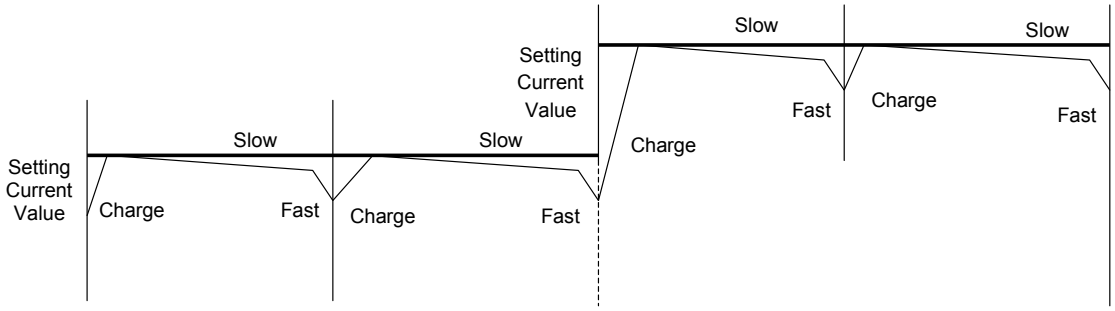
"NF" refers to the point at which the output current reaches its setting current value and "RNF" refers to the monitoring timing of the setting current.

The smaller the MDT value, the smaller the current ripple (current wave peak), and the current's decay capability will fall.

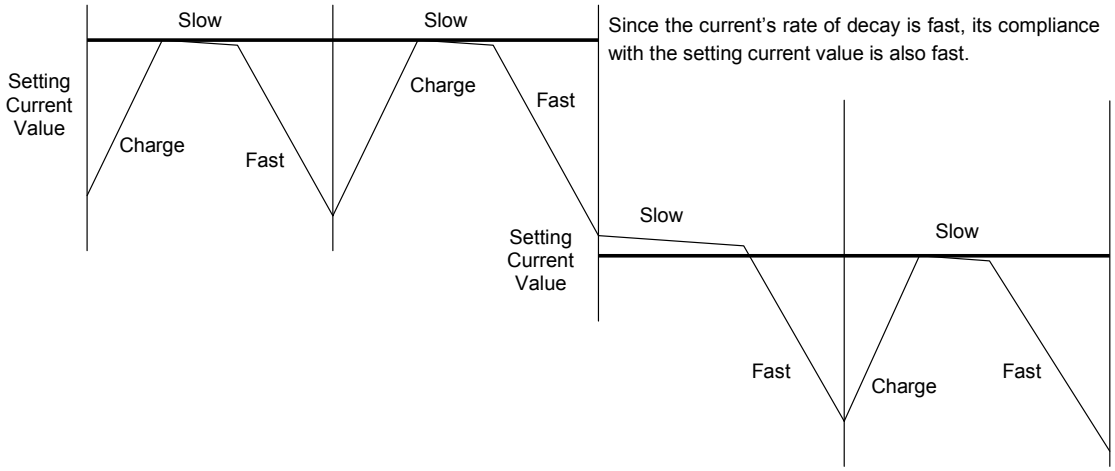


2. Current Control Modes (Decay Mode effect)

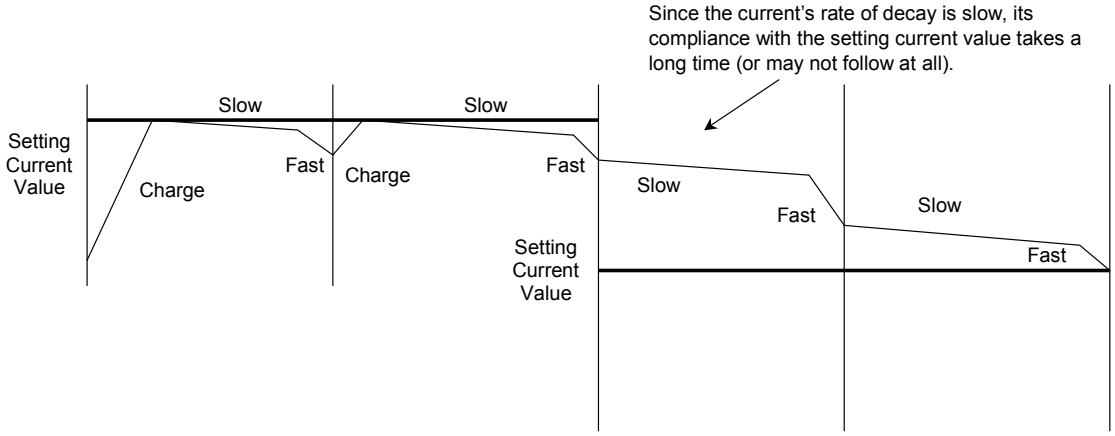
- Direction in which current value increases (sinusoidal wave)



- Direction in which sinusoidal wave decreases
  (when a high decay ratio (MDT%) is used in Mixed Decay mode)



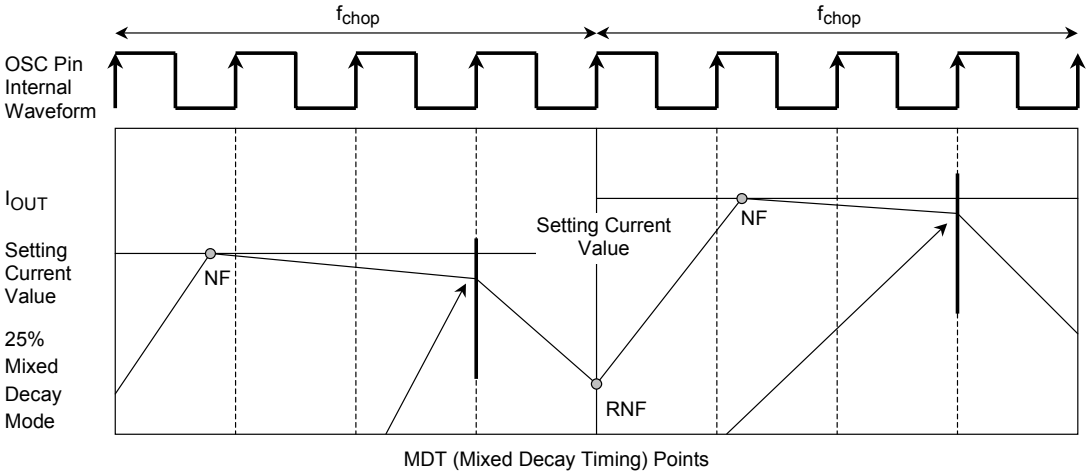
- Direction in which sinusoidal wave decreases
  (when a low decay ratio (MDT%) is used in Mixed Decay mode)



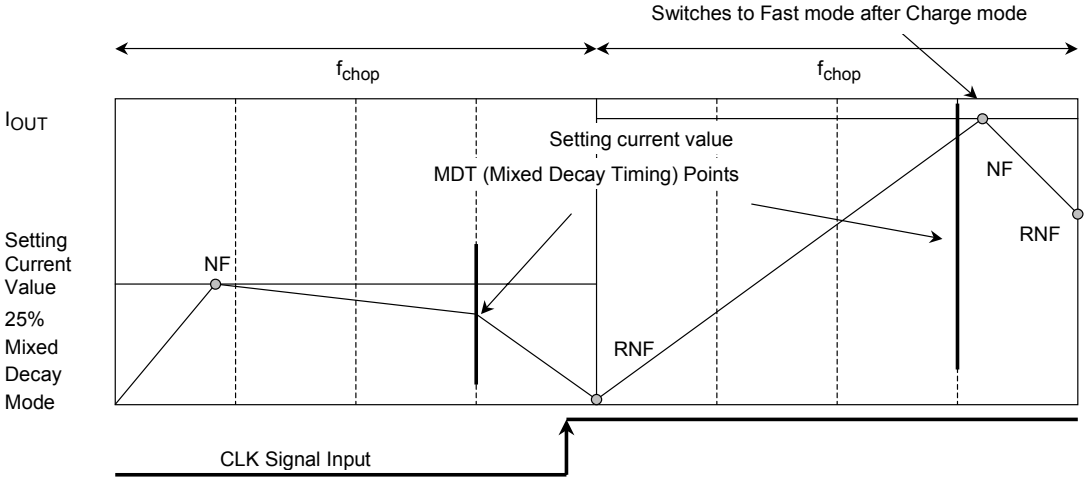
During Mixed Decay mode and Fast Decay mode, if the setting current value < output current at RNF: current monitoring point, the Charge mode at the next chopping cycle will disappear and the pattern will change to Slow + Fast Mode (Slow → Fast occurs at MDT). (In reality, a charge is applied momentarily to confirm the current.)

Note: These figures are intended for illustrative purposes only. If designed more realistically, they would show transient response curves.

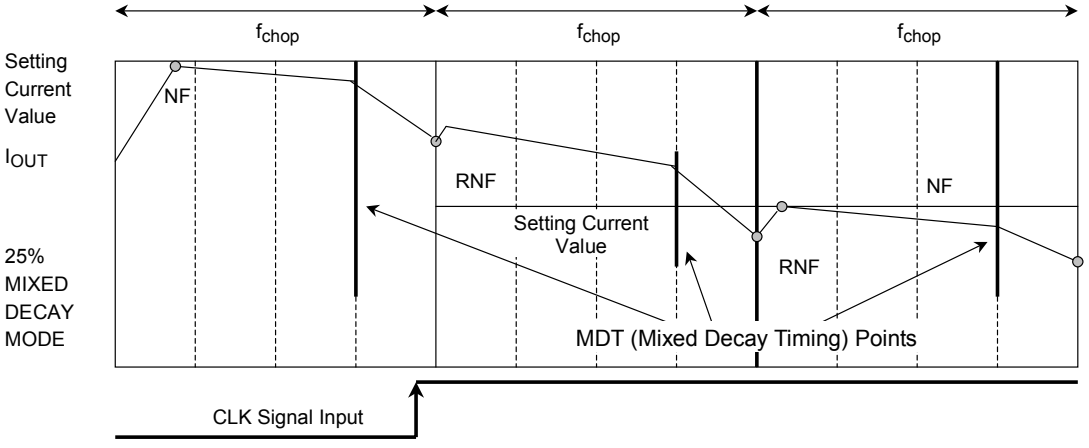
3. Mixed Decay Mode Waveform (Current Waveform)



- When the NF points come after mixed decay timing



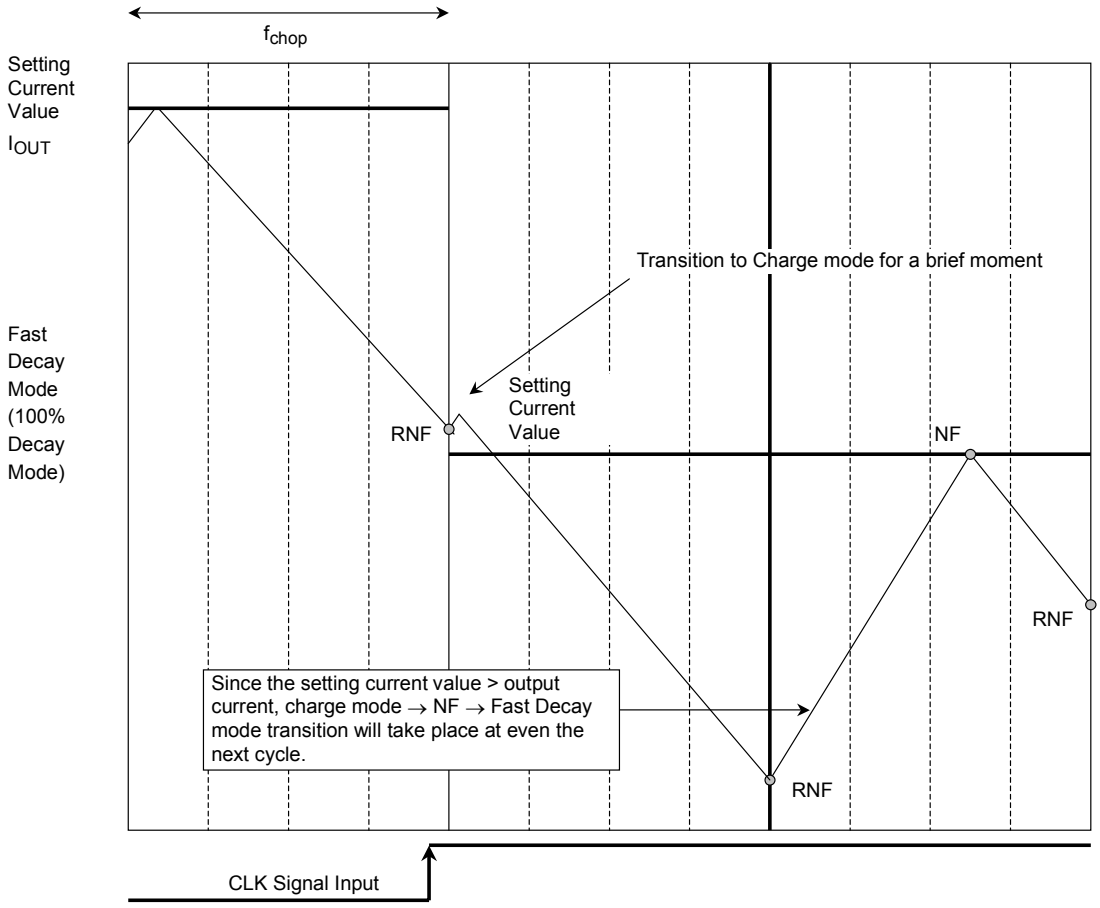
- When the output current value > setting current value in mixed decay mode



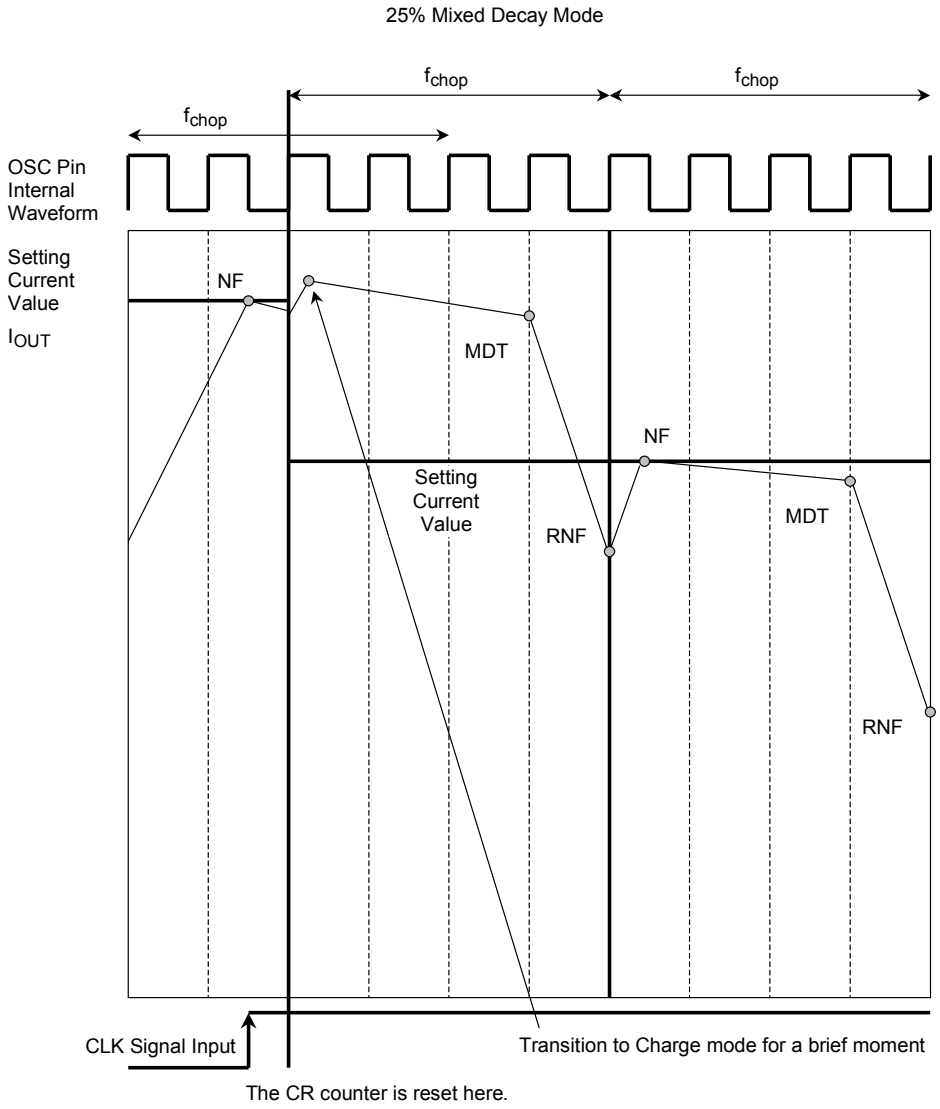
*: Even if the output current rises above the setting current at the RNF point, a charge is applied momentarily to confirm the current.

4. Fast Decay Mode Waveform

After the current value set by RRS, torque or other means is attained, the output current to load will make the transition to full regenerative mode.



5. CLK Signal and Internal CR CK Output Current Waveform (when the CLK signal is input in the middle of Slow mode)



When the CLK signal is input, the Chopping Counter (OSC Counter) is forcibly reset at the timing of the OSC.

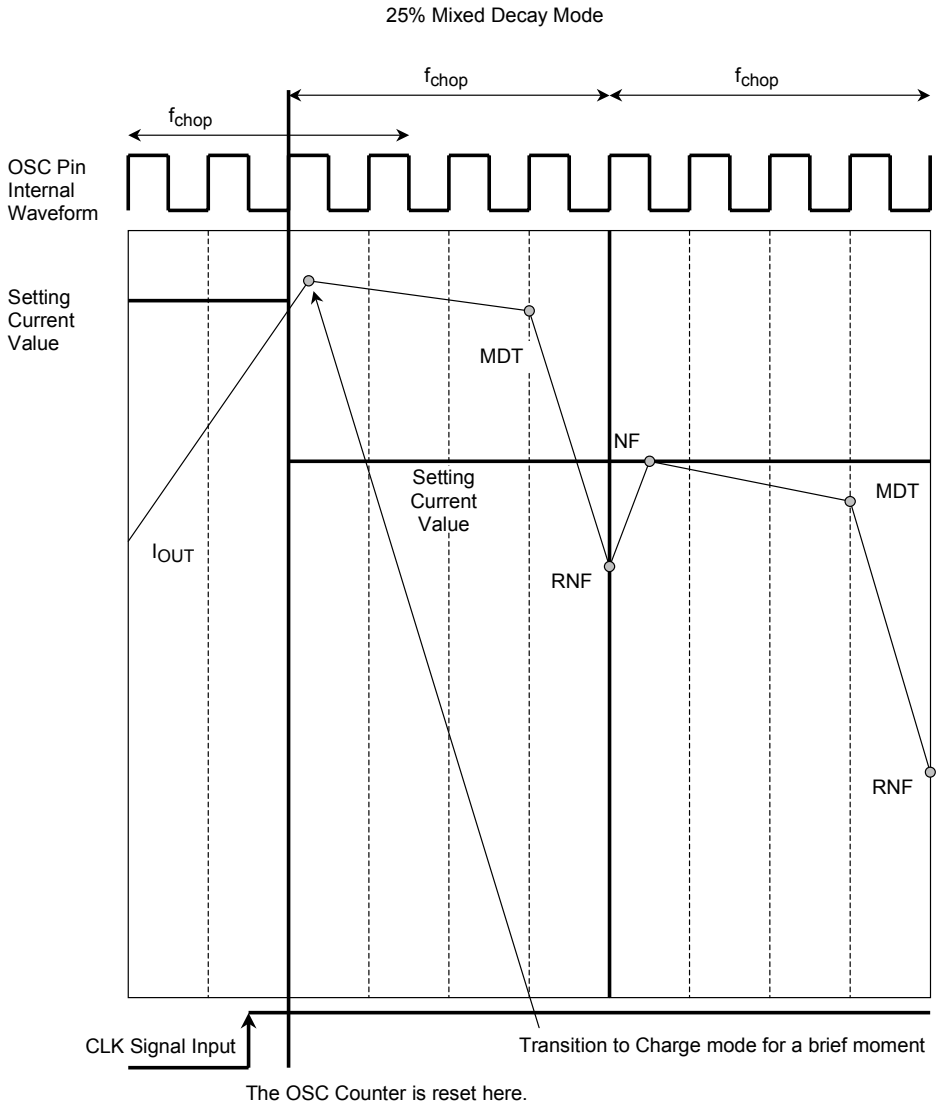
As a result, the response to input data is fast in comparison to methods that don't reset the counter.

The delay time is one OSC cycle: 10 ms @100 kHz Chopping using the Logic Block logic value.

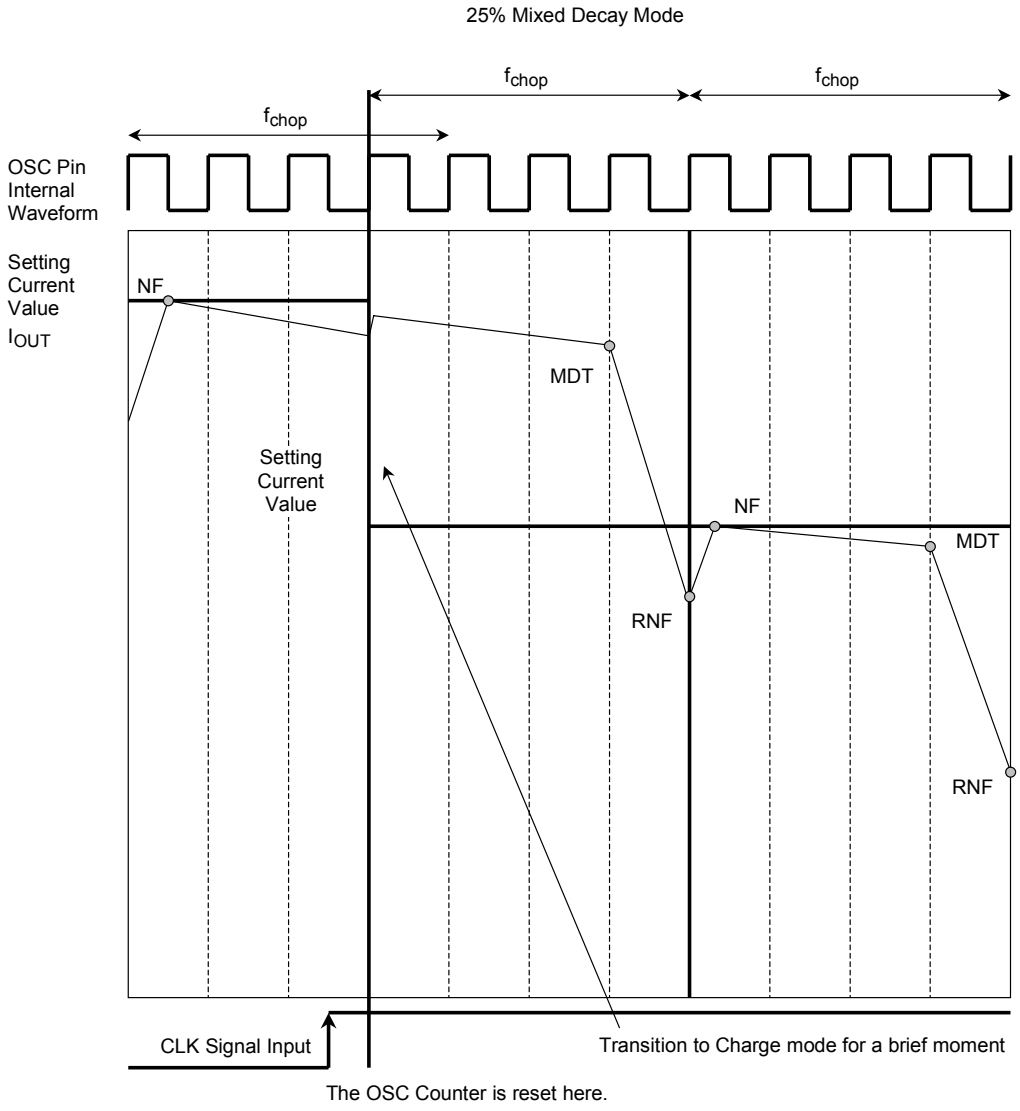
After the OSC Counter is reset by CLK signal input, the transition is invariably made to Charge mode for a brief moment to compare the current.

Note: Even in Fast Decay Mode, the transition is invariably made to Charge mode for a brief moment to compare the current.

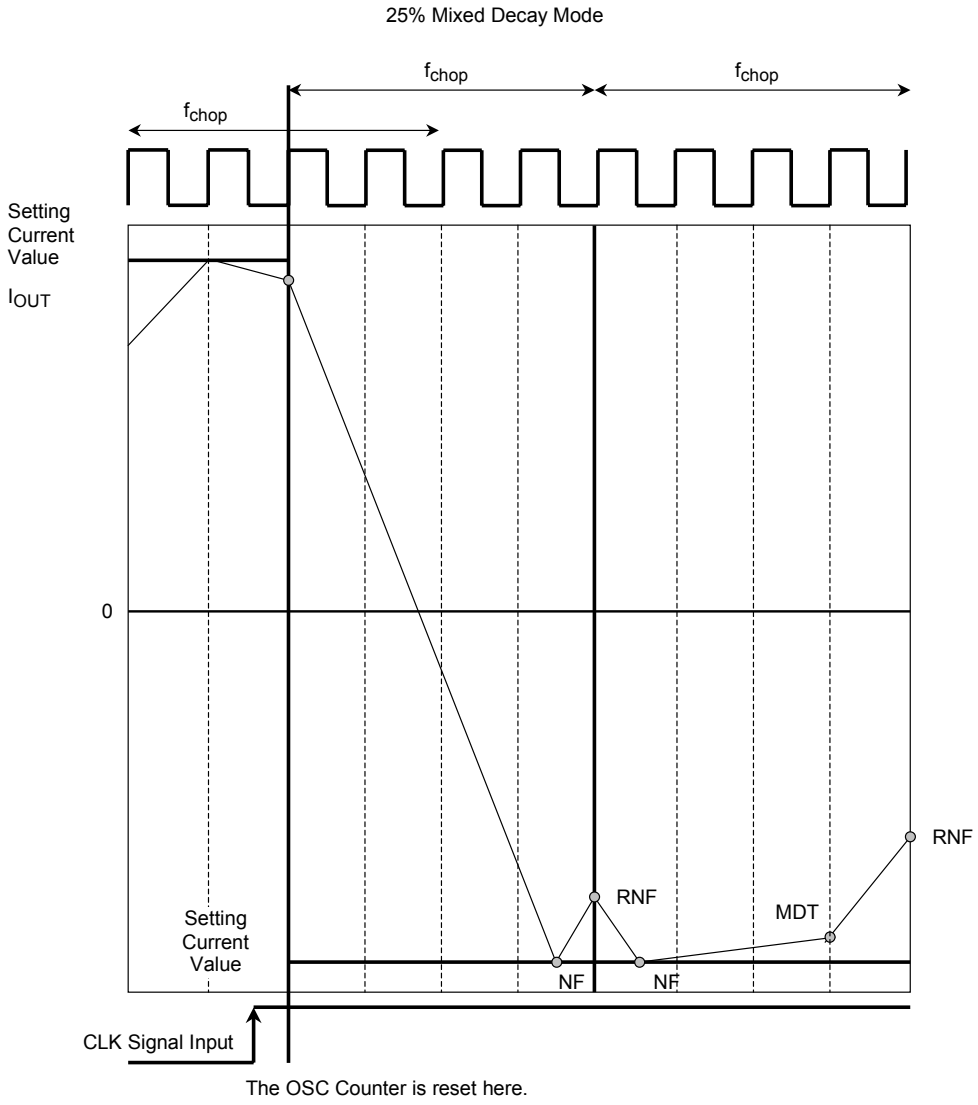
6. CLK Signal and Internal OSC Output Current Waveform
(when the CLK signal is input in the middle of Charge mode)



7. CLK Signal AND Internal OSC Output Current Waveform (when the CLK signal is input in the middle of Fast mode)



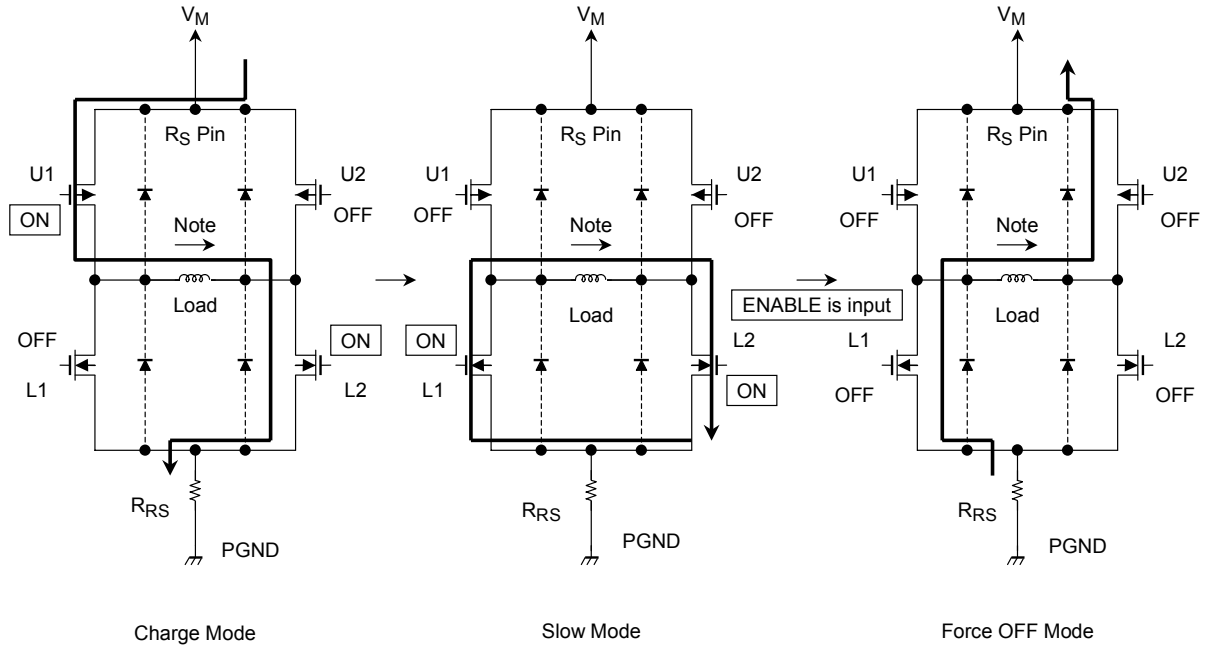
8. Internal OSC Output Current Waveform when Setting Current is Reverse
(when the CLK signal is input using 2-phase excitation)



Current Draw-out Path when ENABLE is Input in Mid Operation

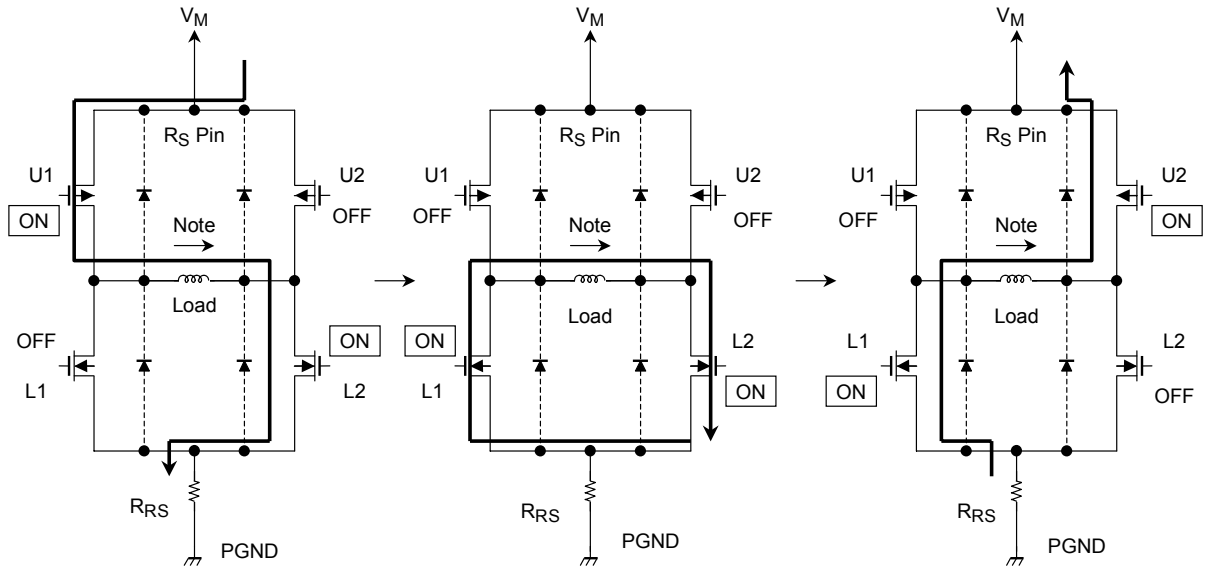
When all the output transistors are forced OFF during Slow mode, the coil energy is drawn out in the following modes:

Note: Parasitic diodes are indicated on the designed lines. However, these are not normally used in Mixed Decay mode.



Normally, when the energy of the coil is drawn out, each transistor is turned ON and the power flows in the opposite-to-normal direction; as a result, the parasitic diode is not used. However, when all the output transistors are forced OFF, the coil energy is drawn out via the parasitic diode.

Output Stage Transistor Operation Mode



Charge Mode Slow Mode Fast Mode

Output Stage Transistor Operation Functions

CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above chart shows an example of when the current flows as indicated by the arrows in the above figures. If the current flows in the opposite direction, refer to the following chart:

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Measurement Waveform

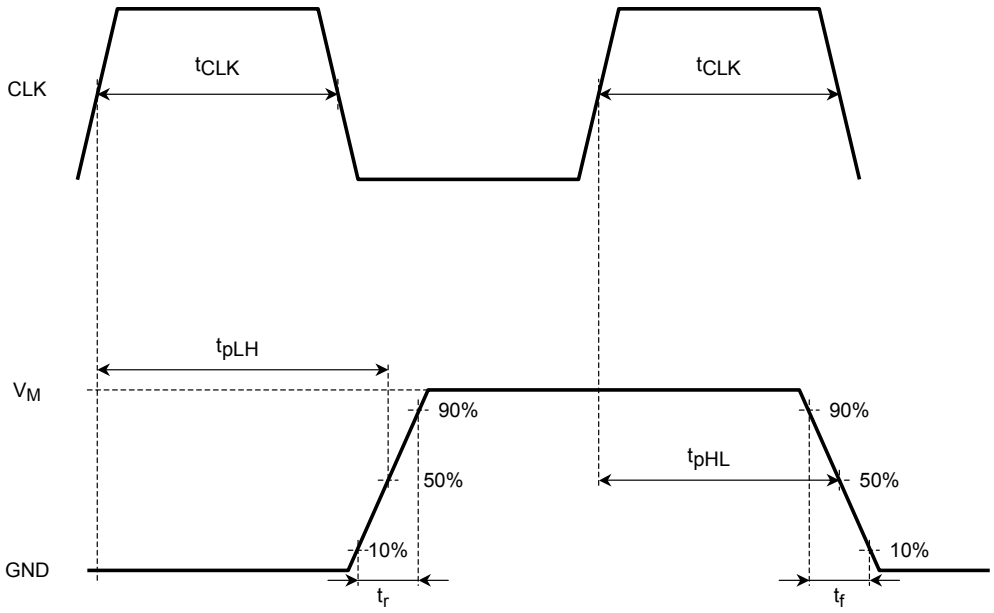
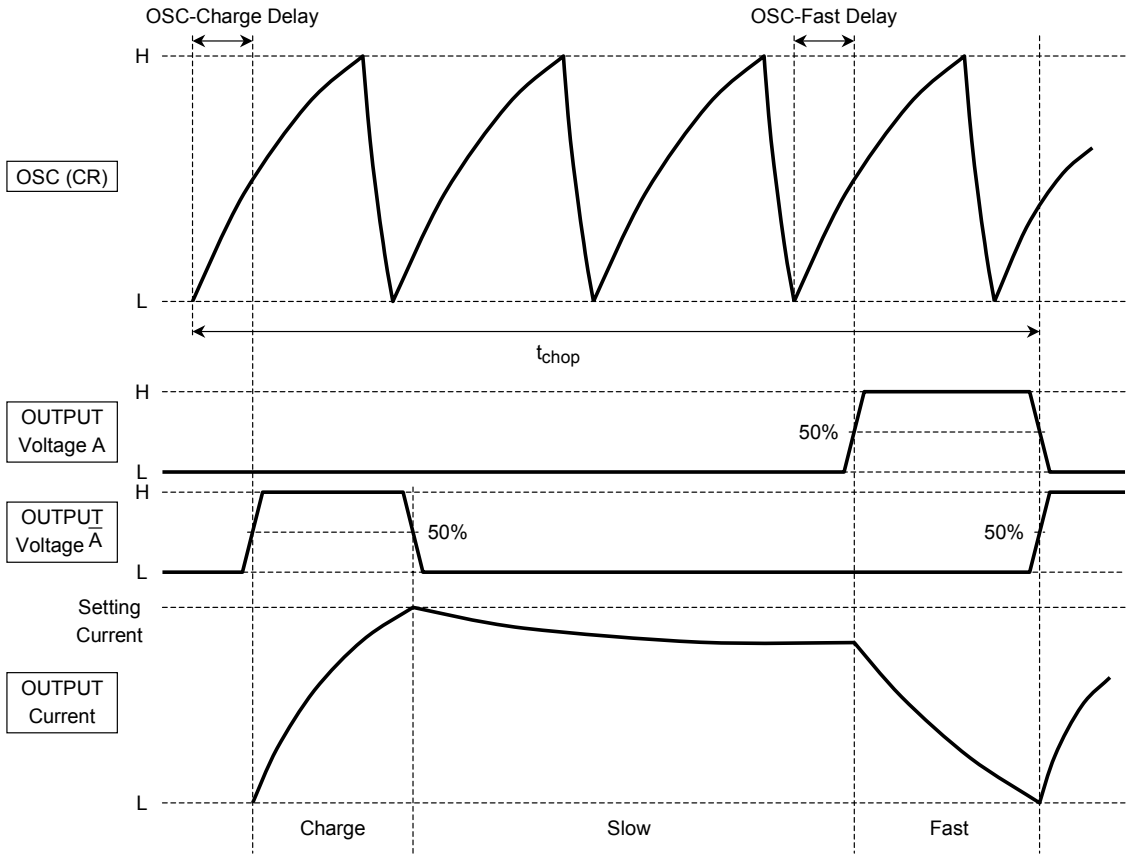


Figure 1 Timing Waveforms and Names



OSC Charge Delay:

When the OSC waveform is converted to an internal OSC waveform, the rising level of the OSC waveform is used. As a result, there is a maximum delay of 1.25 ns (@ fchop = 100 kHz: f_{OSC} = 400 kHz) that occurs between the OSC waveform and internal OSC waveform.

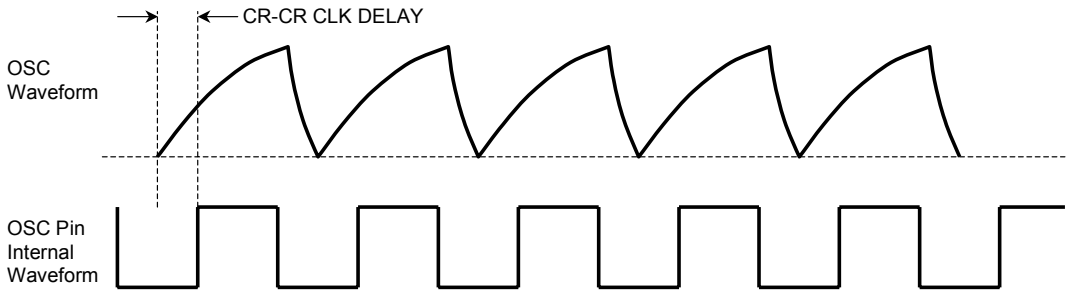
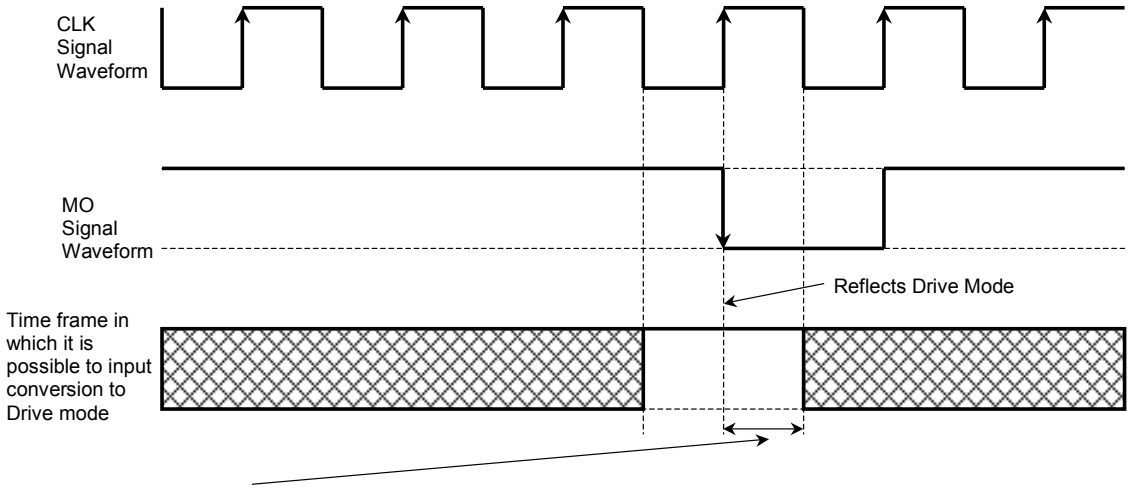
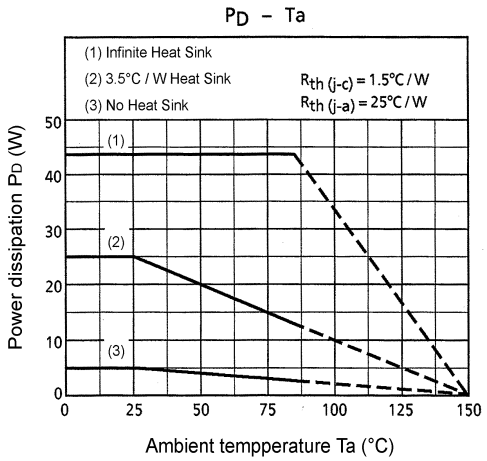


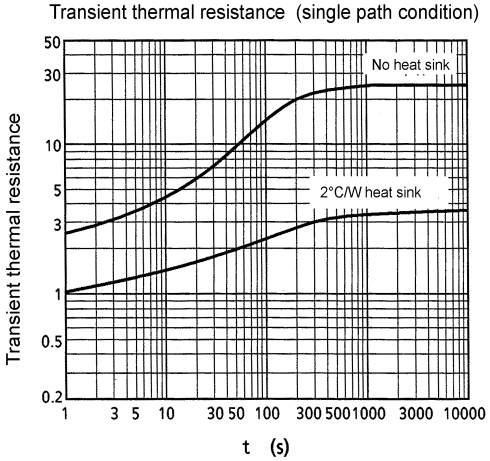
Figure 2 Timing Waveforms and Names (CR and Output)

Recommended Drive Mode Toggle Point



If you wish to toggle the Drive mode forcibly during MO output (while phase data is stopped), a function is needed to set /RESET = L and initialize the electrical angle.

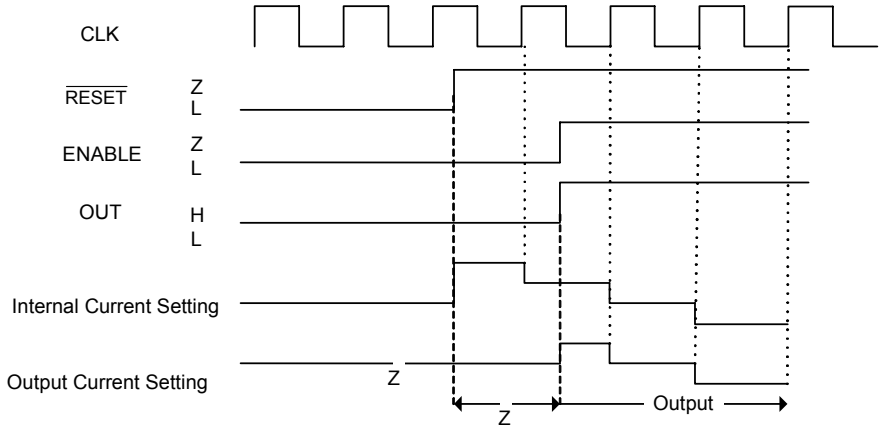




1. How to Turn on the Power

Turn on V_{DD}. When the voltage has stabilized, turn on $V_{MA/B}$.
In addition, set the Control Input pins to Low when inputting the power.
(All the Control Input pins are pulled down internally.)

＜Recommended Control Input Sequence＞



2. Calculating the Setting Current

To perform constant-current operations, it is necessary to configure the base current using an external resistor. If the voltage on the NFA (B) pin is 0.5 V (with a torque of 100%) or greater, it will not charge.

Ex.: If the maximum current value is 1 A, the external resistance will be 0.5 W.

3. PWM Oscillator Frequency (External Condenser Setting)

An external capacitor connected to the OSC pin is used to internally generate a saw tooth waveform. PWM is controlled using this frequency. Toshiba recommends 100 to 3300 pF for the capacitance, taking variations between ICs into consideration.

4. Power Dissipation

The IC power dissipation is determined by the following equation (where the Schottky diode is connected between the output pin and GND):

$P = V_{DD} \times I_{DD} + V_M \times I_M + I_O (t_{ON} \times VSAT{-}U + VSAT{-}L)$
$t_{ON} = T_{ON}/T_S$ (PWM control ON duty).

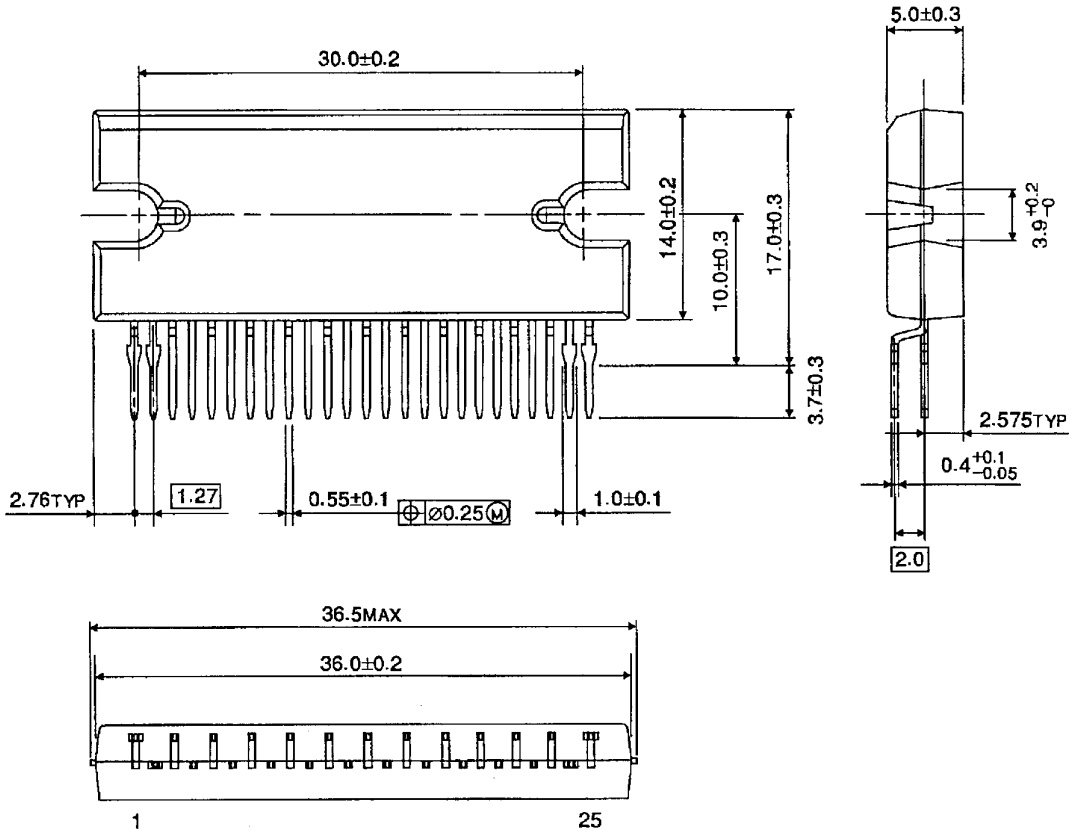
The higher the ambient temperature, the smaller the power dissipation.
Check the PD-Ta curve, and be sure to design the heat dissipation with a sufficient margin.

5. Heat Sink Fin Processing

The IC fin (rear) is electrically connected to the rear of the chip. If current flows to the fin, the IC will malfunction. If there is any possibility of a voltage being generated between the IC GND and the fin, either ground the fin or insulate it.

Package Dimensions

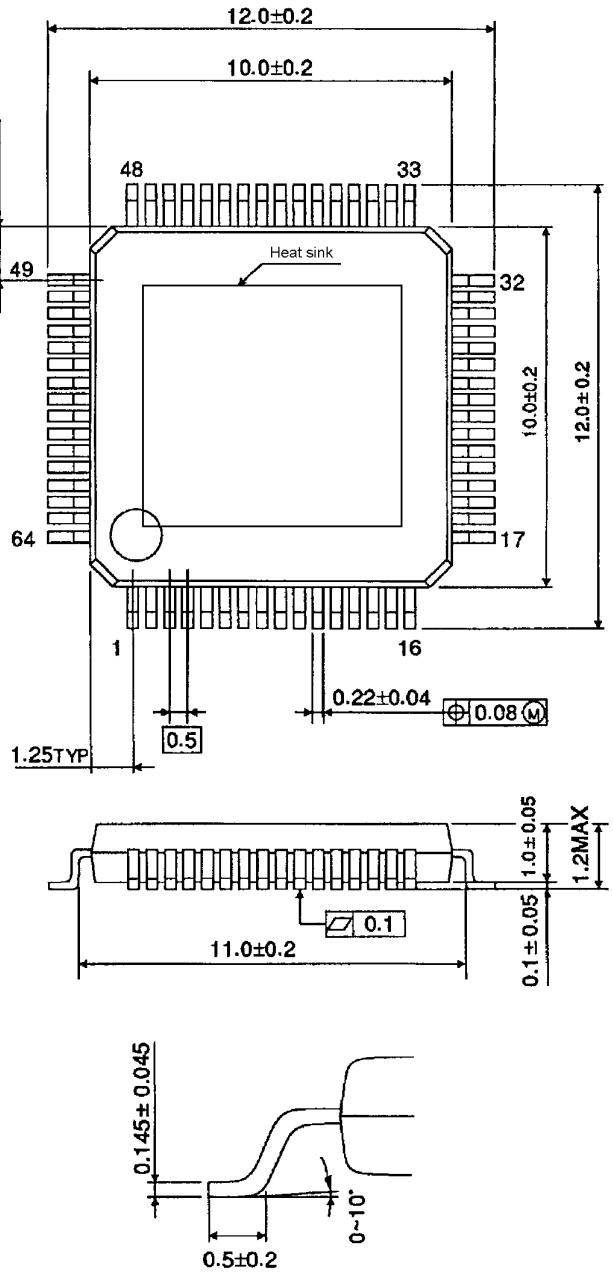
HZIP25-P-1.27 Unit : mm



Weight: 9.86 g (typ.)

Package Dimensions

HQFP64-P-1010-0.50 Unit : mm



Weight: 0.26 g (typ.)

Note: The rear heat sink block will be 5.5 mm × 5.5 mm. (PROVISIONAL)

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